REMARKS

Claims 1 – 28 remain in the application. Claims 1 – 28 stand rejected. Election of claims 1 – 28 is hereby affirmed as required in the office action. Claims 29 – 38 are withdrawn as being drawn to a non-elected invention. The rejection of claims 1 – 28 is respectfully traversed.

Claim 25 is amended herein for grammatical reasons, i.e., to insert a period at the end thereof. No new matter is added.

Claims 1 – 4, 9 – 15 and 18 – 20 are rejected under 35 U.S.C. §103(a) over U.S. Patent Publication No. 2004/00724 to Murthy et al. in view of U.S. Patent No. 6,437,404 to Xiang et al. Claims 5, 7, 16 and 21 are rejected under 35 U.S.C. §103(a) over the combination of Murthy et al. and Xiang et al. in further view of U.S. Patent No. 6,743,680 to Yu. Claims 6 and 22 – 26 are rejected under 35 U.S.C. §103(a) over the combination of Murthy et al., Xiang et al. and Yu in further view of "Microchip Fabrication" to Van Zandt. Claims 17, 27 and 28 are rejected under 35 U.S.C. §103(a) over the combination of (presumably Murthy et al. and) Xiang et al. in further view of U.S. Patent No. 6,271,094. Other than the indication on page 1 of the Office Action that claims 1 – 28 are rejected, no specific rejection, rationale or discussion is provided regarding claim 8. Accordingly, any subsequent rejection of claim 8 could not be final. The rejection of claims 1 – 28 is respectfully traversed.

It is asserted that the devices of Murthy et al. may be modified with elements of the devices of Xiang et al. to result in the present invention in general and, in particular, as claimed in claims 1 and 18. In support for combining it is asserted that, "[I]t would have been obvious ... to modify the semiconductor of Murthy to include the use of a source and drain substantially thicker than said thin channel as disclosed in Xiang because it aids in reducing high parasitic resistance... ." To provide further support for

the combination, it is asserted that "Murthy and Xiang are both from the same field of endeavor, [and that therefore] the purpose disclosed by Xiang would have been recognized in the pertinent art of Murthy."

As recited in claims 1 and 18, the present invention is a FET and an IC including the FETs. The FET includes a thin channel of a thin semiconductor layer with a gate above the channel and source/drain regions in recesses at either end of the thin channel. The source/drain regions are substantially thicker than the thin channel with a source/drain extension between the thin channel and each source/drain region. Further, the FETs are self aligned; each source/drain extension and corresponding source/drain region is aligned to the gate and the thin channel. Self alignment is a result of forming the preferred embodiment devices. Although the method claims for forming such a device have been withdrawn, paragraphs 24 – 35 provide a detailed description of how such self-aligned preferred embodiment devices may be formed.

Murthy et al. teaches "an ultra-thin body epitaxial layer that forms an embedded junction with a channel that has a length dictated by an undercut under the gate stack" as recited in the Abstract. The Murthy et al. device begins on a "substrate 12 [that] has an SOI insulator layer 14, and an SOI silicon layer 16." Paragraph 24. The device itself is formed in and from the surface SOI silicon layer 16 with the underlying SOI insulator layer 14 and substrate 12 remaining substantially unchanged. *See*, Figures 1 – 14. The channel 36 is defined by undercutting the SOI silicon layer 16 at either side of gate 22 and growing an ultra-thin epi layer 52 on the surface to fill the self-aligned undercuts 34 with a raised epi tip 56 forming in the undercuts. *See, e.g.*, paragraphs 39 – 40. The epi tips 56 may or may not be higher than the surface of the channel 36. *Id.* Since the ultra-thin epi layer 52 forms a junction 58 with the channel 36, it must be assumed that the epi is formed of in situ doped semiconductor material, i.e., it is not diffused. *See, e.g.*, paragraphs 43 – 47. Murthy et al. has no mention of diffusing dopant or diffusion. Thus, it is very apparent that Murthy et al. is relying on the junction formation from depositing the doped semiconductor material such that it contacts the channel 36. Instead, Murthy et

al. includes a self-aligned source/drain junctions 58 butted to the ends of the channel 36. It is, therefore, clear extensions are undesired between the Murthy et al. channel 36 and the ultra-thin epi layer 52. Extensions would appear to frustrate the purpose of Murthy et al.

Xiang et al. teaches a "fully-depleted semiconductor-on-insulator (SOI) transistor" as recited in the Abstract. The device is formed on a solid semiconductor wafer 110. Col. 4, lines 48 – 49. A dummy device structure 120 is formed on the solid semiconductor wafer 110. Col. 4, line 54 – col. 5, line 27, *and see*, Figure 3. Oxygen 144 is implanted into the solid semiconductor wafer 110 with the dummy device structure 120 acting as a profile mask. Col. 5, lines 33 – 45 *and see*, Figure 4. Thereafter, the wafer 110 is annealed, converting the implanted oxygen into oxide such that a non-planar buried oxide layer 164 is formed. *Id*, lines 46 – 56 *and see*, Figure 5. Thus, the solid semiconductor wafer 110 has been converted into a layered SOI wafer profiled by the dummy layer. Next, a dummy spacer 128, 130 portion of the dummy device structure 120 is removed and extensions and source/drain regions 182, 184 are formed simultaneously on either side of the dummy gate 134. Col. 5, line 57 – col. 6, line 6 *and see*, Figures 6 – 8. Silicide 202, 204 is formed on source/drain regions 182, 184. Col. 6, lines 12 – 34 *and see*, Figures 2 (26, 28) and 9. Thereafter, the dummy gate 134 is removed, gate oxide 58 and the device gate 56 are formed above the channel and on the source/drain extensions 50 – 52. *Id*, lines 35 – 52. Accordingly, the Xiang et al. device 12 is in no way self aligned.

The Murthy et al. FET formed from the surface layer is completely incompatible with the subsurface structure in Xiang et al.

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation,... . Second, there **must be a reasonable expectation of success.** Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination **and the reasonable expectation of success** must both be

> found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (emphasis added.)

Thus, to suggest the invention, the references relied upon must show how to combine features from these two very different devices and method of making the devices to result in the present invention. One certainly would not be inclined to implant oxygen into the Murthy et al. SOI wafer. That would not result in thickened source/drain regions. Neither would one be inclined to remove the Xiang et al. source/drain regions to redeposit a thicker, rather than an ultra-thin epi layer at the extensions. Neither of Murthy et al. or Xiang et al. give any indication of how self-alignment could be maintained with any attempted combination. If Murthy et al. were being combined with Xiang et al. to suggest forming something on the surface of the wafer, e.g., the gate, perhaps the applicants would be inclined to agree that the combination was suggested. However, that is not what is being asserted. Thus, neither Murthy et al. or Xiang et al. provide any indication of any likelihood of success of modifying each other below gate level and, therefore, the combination is insufficient to establish a *prima facie* case of obviousness.

Accordingly, because the combination of Murthy et al. and Xiang et al. does not result in the present invention; because such a combination would frustrate the purpose of either or both of Murthy et al. and Xiang et al.; and, because there is no likelihood of any success of the combination; the combination of Murthy et al. and Xiang et al., alone or in further combination with any reference of record, does not make the present invention, as claimed in claims 1 and 18, unpatentably obvious under 35 U.S.C. §103(a). Further, because dependent claims include all of the differences with the prior art as the claims from which they depend, claims 2 – 17 and 19 – 28, which depend from claims 1 and 18, are not unpatentably obvious over Murthy et al. and Xiang et al. under 35 U.S.C. §103(a). Reconsideration and withdrawal of the rejection of claims 1 – 28 under 35 U.S.C. §103(a) is respectfully solicited.

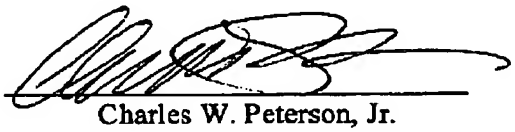
The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance for the reasons

set forth above, the applicants respectfully request that the Examiner reconsider and withdraw the rejection of claims 1 – 28, under 35 U.S.C. §103(a) and allow the application to issue.

Should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 09-0458 and advise us accordingly.

Respectfully Submitted,



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